REMARKS

In the Office Action mailed May 4, 2005, claims 1-2, 4-6, 10, 23 and 28 are rejected under 35 USC §102(b) as being anticipated by Akao et al. (US Patent 5,307,464, hereinafter "Akao"). Claims 1-6, 10-13, 23 and 28 are rejected under 35 USC §103(a) as being obvious over "The Programmable Logic Data Book 2000" in view of Akao. Finally, claims 3, 11-13, 24-27 and 29-32 are rejected under 35 USC §103(a) as being obvious in view of Akao or "The Programmable Logic Data Book 2000" in view of Akao and further in view of Applicant's disclosure in Paragraphs [0015] and [0016].

I. Akao Fails to Disclose or Suggest an Integrated Circuit having a Configurable Peripheral Device as Claimed

In response to the rejection of claims 1-2, 4-6, 10, 23 and 28 as being anticipated by Akao, Applicant respectfully requests reconsideration. Akao fails to disclose the elements for which it is cited for each of the independent claims 1 and 6, and that the claims clearly distinguish over Akao, alone or in combination with other cited references. In particular, Akao fails to disclose or suggest (i) a configurable peripheral device comprising a configurable logic block, (ii) a bus connecting the processor core and the configurable peripheral device without using a sub-processor, or (iii) a programmable routing matrix as claimed. While it is suggested in the "Response to Arguments" section on pages 6 and 7 of the current Office Action that it is unclear how something that provides functional elements for constructing logic differs from an EPROM, a RAM, or a PLD, Applicant notes that the claims recite a configurable logic block "having circuitry capable of implementing a plurality of logic functions." Applicant submits that one skilled in the art would not consider an ERPOM or RAM to be a configurable logic block having circuitry capable of implementing a plurality of logic functions as claimed. That is, RAM3 and ROM (EPROM) 4 are memory elements, not configurable logic blocks having circuitry capable of implementing a plurality of logic functions as claimed.

Applicant notes that the reference to a PLD on pages 6 and 7 of this Office

Action (i.e. comparing functional elements for constructing logic to a PLD) is inaccurate. In the Office Action mailed on December 23, 2004, Southgate (U.S. Patent 5,968,161) is cited for teaching that programmable/configurable logic devices are implemented using various types of programmable devices including an EPPROM. Southgate, which discloses an FPGA, could be implemented with an EPROM. However, as set forth in our response mailed on March 15, 2005, Southgate does not indicate that an EPROM is a programmable logic device. That is, Applicant was stating that a configurable logic block differs from an EPROM or RAM, but was not making any comparison of a configurable logic block to a PLD.

However, Applicant further submits that Akao clearly fails to disclose the bus coupled between the processor core and the configurable peripheral device as claimed. It is suggested in the Office Action that Akao discloses a bus connecting the processor core 2 and the configurable device without a sub-processor in the embodiment where a PLA or PLD is implemented in place of sub-processor 5 as disclosed in col. 32, lines 23-30 and col. 33, lines 46-58. However, Applicant respectfully submits that col. 32, lines 23-30 and col. 33, lines 46-58 of Akao fail to disclose or suggest that a PLA or PLD is used in place of sub-processor 5. Col. 32, lines 23-30 of Akao states that operation control signals "can also be generated by a wired logic configuration utilizing PLDs [or] PLAS." Similarly, col. 33, lines 46-58, indicates that the scope of the invention is not limited to such a sub-processor, but that "[i]nstead, a programmable logic array can also be configured by using non-volatile memory elements." Applicant respectfully submits that there is no teaching or suggestion that a PLD or PLA is coupled to a processor core without using a sub-processor. That is, there is no teaching or suggestion in Akao that a PLD or PLA replaces the sub-processor 5. While one function of the sub-processor of Akao is to generate information defining peripheral functions, the sub-processor provides other functions described in Akao. Further, there is no teaching or suggestion that a PLD or PLA is on the integrated circuit as claimed by Applicant.

Finally, Applicant submits that Akao fails to disclose or suggest a programmable routing matrix coupled to the configurable logic block as claimed. It is suggested in the Office Action that the RAM array address control circuit for selecting

column and row addresses shown in Figs. 6 and 15 of Akao discloses a programmable routing matrix. However, Fig. 6 describes the MicroROM (EPROM) 13 of the sub-processor 5 (shown in Fig. 2). Accordingly, any reading of the claim suggesting that a PLD or PLA is used in place of the sub-processor could not also require including the sub-processor, as would be required if relying on the disclosure of Fig. 6 of Akao. Similarly, Fig. 15 is a block diagram of the ROM 4. However, Applicant respectfully submits that the ROM 4 could not be both the configurable peripheral device and the programmable routing matrix. Accordingly, Applicant respectfully submits that independent claims 1 and 6, and their dependent claims, clearly distinguish over Akao.

II. Any Combination of "The Programmable Logic Data Book 2000" with Akao would Fail to Disclose or Suggest an Integrated Circuit having a Configurable Peripheral Device as Claimed

It is suggested in the Office Action that it is well known "to implement a single chip microprocessor having embedded configurable hardware logic with a processor (CPU 2) to provide various peripheral functions" according to col. 1, lines 29-65 of Akao. However, col. 1, lines 29-65 does not state that a single chip microprocessor has embedded configurable hardware logic to provide peripheral functions. Rather, col. 1, lines 29-65 states that:

> "the single chip microcomputer has got to embed a variety of hardware peripheral circuits configurable also as logic external to the CPU such as interface circuits, timers, counters, and serial input/output control circuits. However, even though software stored in EPROM program memory can be modified, the hardware peripheral circuits embedded in such a microcomputer, particularly functional portions of the hardware logic, are fixed."

Accordingly, Akao teaches the hardware peripheral circuits are configurable as logic "external to the CPU." That is, Akao is not stating that the hardware peripheral circuits are configurable logic, but rather that the hardware peripheral circuits are configured as logic external to the CPU. This interpretation is reinforced by the following sentence, which expressly states that the hardware circuits embedded in such a

microcomputer are fixed. In order to overcome this problem of fixed hardware, Akao teaches "implementing required peripheral functions through software." Accordingly, claims 1-6, 10-13, 23 and 28 (which includes independent claims 1 and 6) should be allowable over any combination of "The Programmable Logic Data Book 2000" and Akao. That is, neither reference discloses a configurable peripheral device, the bus coupling the processor core to the configurable peripheral device, or the configurable routing matrix as claimed for the same reasons set forth above with respect to Akao.

III. Akao or Any Combination of "The Programmable Logic Data Book 2000" in view of Akao and Applicant's Paragraphs 15-16 would Fail to Disclose or Suggest an Integrated Circuit having a Configurable Peripheral Device

Applicant respectfully submits that Akao or any combination of "The Programmable Logic Data Book 2000" in view of Akao and Applicant's Paragraphs 15-16 would fail to disclose or suggest any of the dependent claims 3, 11-13, or 24-27 for the same reason that Akao fails to disclose or suggest the subject matter of the their respective independent claims. Similarly, Applicant respectfully submits that Akao fails to disclose or suggest a universal asynchronous receiver transmitter circuit having a baud rate generator implemented in a configurable logic block, as well as the bus or the programmable routing matrix of independent claim 29 and its dependent claims 30-32, for the same reasons set forth above. Finally, Applicant respectfully submits that any combination of "The Programmable Logic Data Book 2000" in view of Akao and Applicant's Paragraphs 15-16 would lead to Applicant's claims 29-32. That is, none of the references discloses or suggests a universal asynchronous receiver transmitter circuit having a baud rate generator implemented in a configurable logic block. Accordingly, claims 3, 11-13, 24-27 and 29-32 should be allowable over Akao or any combination of "The Programmable Logic Data Book 2000" in view of Akao and Applicant's Paragraphs 15-16.

IV. Conclusion

All claims should be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the Applicant's attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

Kim Kanzaki, Ph.D.
Attorney for Applicant
Reg. No. 37,652

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Appeal Brief – Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on June 27, 2005.

Pat Slaback _____
Name *Signature*